L Number	Hits	Search Text	DB	Time stamp
1	238	(first adj2 power adj2 rail)	USPAT; EPO; JPO; DERWENT	2004/05/27 11:30
2	190	(first adj2 power adj2 rail) and (second adj2 power adj2 rail)	USPAT; EPO; JPO; DERWENT	2004/05/27 11:30
3	23	(first adj2 power adj2 rail) and (second adj2 power adj2 rail) and (third adj2 power adj2 rail)	USPAT; EPO; JPO; DERWENT	2004/05/27 11:30
4	35	(first adj2 power adj2 rail) and (second adj2 power adj2 rail) and (latch$3 or flip-flop$1)	USPAT; EPO; JPO; DERWENT	2004/05/27 11:31
5	35	(first adj2 power adj2 rail) and (second adj2 power adj2 rail) and (latch$3 or flip-flop$1) and (logic or circuit$1 or core$1)	USPAT; EPO; JPO; DERWENT	2004/05/27 11:32
6	9	(first adj2 power adj2 rail) and (second adj2 power adj2 rail) and (latch$3 or flip-flop$1) and (logic or circuit$1 or core$1) and test$3	USPAT; EPO; JPO; DERWENT	2004/05/27 11:34
7	9	(first adj2 power adj2 rail) and (second adj2 power adj2 rail) and (latch$3 or flip-flop$1) and (logic or circuit$1 or core$1) and (test$3 or stress$3)	USPAT; EPO; JPO; DERWENT	2004/05/27 11:35
8	1406	(first adj2 power) and (second adj2 power) and (latch$3 or flip-flop$1) and (logic or circuit$1 or core$1) and (test$3 or stress$3)	USPAT; EPO; JPO; DERWENT	2004/05/27 11:35
9	1406	(first adj2 power) and (second adj2 power) and (latch$3 or flip-flop$1) and (logic$1 or circuit$1 or core$1) and (test$3 or stress$3)	USPAT; EPO; JPO; DERWENT	2004/05/27 11:37
10	10	(first adj2 power) same (second adj2 power) same (latch$3 or flip-flop$1) same (logic$1 or circuit$1 or core$1) same (test$3 or stress$3)	USPAT; EPO; JPO; DERWENT	2004/05/27 11:39
11	90	((first adj2 power) same (second adj2 power) same (latch$3 or flip-flop$1) same (logic$1 or circuit$1 or core$1)) and (test$3 or stress$3)	USPAT; EPO; JPO; DERWENT	2004/05/27 11:41
12	3185	(first adj2 (latch or flip-flop)) and (second adj2 (flip-flop or latch)) and (third adj2 (flip-flop or latch))	USPAT; EPO; JPO; DERWENT	2004/05/27 11:42
13	30	(first adj2 (latch or flip-flop)) and (second adj2 (flip-flop or latch)) and (third adj2 (flip-flop or latch)) and (core near3 logic) and clock$3	USPAT; EPO; JPO; DERWENT	2004/05/27 11:44
14	24	(first adj2 (latch or flip-flop)) and (second adj2 (flip-flop or latch)) and (third adj2 (flip-flop or latch)) and (core near3 logic) and clock$3 and test$3	USPAT; EPO; JPO; DERWENT	2004/05/27 11:50
15	168	first adj2 ((core near3 logic) or (combinatorial adj2 logic))	USPAT; EPO; JPO; DERWENT	2004/05/27 11:51
16	100	(first adj2 ((core near3 logic) or (combinatorial adj2 logic))) and (second adj2 ((core near3 logic) or (combinatorial adj2 logic)))	USPAT; EPO; JPO; DERWENT	2004/05/27 11:52
17	22	(first adj2 ((core near3 logic) or (combinatorial adj2 logic))) and (second adj2 ((core near3 logic) or (combinatorial adj2 logic))) and (third adj2 ((core near3 logic) or (combinatorial adj2 logic)))	USPAT; EPO; JPO; DERWENT	2004/05/27 11:52

18	14	(first adj2 ((core near3 logic) or (combinatorial adj2 logic))) and (second adj2 ((core near3 logic) or (combinatorial adj2 logic))) and (third adj2 ((core near3 logic) or (combinatorial adj2 logic))) and clock$3 and (latch$3 or flip-flop$1)	USPAT; EPO; JPO; DERWENT	2004/05/27 11:53
19	10	(first adj2 ((core near3 logic) or (combinatorial adj2 logic))) and (second adj2 ((core near3 logic) or (combinatorial adj2 logic))) and (third adj2 ((core near3 logic) or (combinatorial adj2 logic))) and clock$3 and (latch$3 or flip-flop$1) and (power or VVD$1 or VVS$1)	USPAT; EPO; JPO; DERWENT	2004/05/27 11:54